

IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A semiconductor device, comprising:
a semiconductor substrate with a trench, the semiconductor substrate comprising a first semiconductor layer of a first conductivity type and a second semiconductor layer disposed above the first semiconductor layer, and the second semiconductor layer including
a first impurity diffusion region of the first conductivity type,
a second impurity diffusion region of a second conductivity type, the second impurity diffusion region and the trench sandwiching the first impurity diffusion region,
a base region of the second conductivity type which faces the first semiconductor layer with the first and second impurity diffusion regions interposed therebetween and is spaced apart from the trench, and
a source region of the first conductivity type which faces the first semiconductor layer with the base region and the second impurity diffusion region interposed therebetween and is spaced apart from the first impurity diffusion region;
a particulate insulating layer filling at least a lower portion of the trench and comprising insulating particles, wherein an average diameter of the insulating particles falls within a range of 100 nm to 500 nm or a range of 100 nm to half a width of opening of the trench; and
a reflowable dielectric layer covering an upper surface of the particulate insulating layer, the insulating particles being stable at a melting point or a softening point of the reflowable dielectric layer;

a gate electrode facing a portion of the base region interposed between the first impurity diffusion region and the source region;

a gate insulating film interposed between the gate electrode and the base region;

a source electrode covering the source region; and

a drain electrode covering the first semiconductor layer, the drain and source electrodes sandwiching the semiconductor substrate.

2. (Original) The device according to claim 1, wherein the reflowable dielectric layer comprises silicate glass doped with impurity.

3. (Original) The device according to claim 1, further comprising a barrier insulating layer on a sidewall and a bottom surface of the trench.

4. (Original) The device according to claim 1, further comprising a cap insulating layer covering an upper surface of the reflowable dielectric layer and having a melting point or a softening point higher than the melting point or the softening point of the reflowable dielectric layer.

5. (Original) The device according to claim 1, wherein the particulate insulating layer further comprises an insulating binder.

6. (Original) The device according to claim 1, wherein an upper surface of the particulate insulating layer is lower than an upper surface of the semiconductor substrate.

7. (Canceled).

8. (Previously Presented) A semiconductor device, comprising:
a semiconductor substrate with a trench; and
a particulate insulating layer filling at least a lower portion of the trench and
comprising first and second insulating particles, an average diameter of the second insulating
particles being smaller than an average diameter of the first insulating particles,
wherein the first insulating particles form a first particulate insulating layer, and the
second insulating particles form a second particulate insulating layer covering an upper
surface of the first particulate insulating layer.

9. (Original) The device according to claim 8, further comprising a barrier insulating
layer on a sidewall and a bottom surface of the trench.

10. (Canceled).

11. (Canceled).

12. (Original) The device according to claim 8, further comprising a reflowable
dielectric layer covering an upper surface of the particulate insulating layer, the first and
second insulating particles being stable at a melting point or a softening point of the
reflowable dielectric layer.

13. (Original) The device according to claim 12, further comprising a cap insulating layer covering an upper surface of the reflowable dielectric layer and having a melting point or a softening point higher than the melting point or the softening point of the reflowable dielectric layer.

14. (Original) The device according to claim 8, wherein the particulate insulating layer further comprises an insulating binder.

15. (Original) The device according to claim 8, wherein the average diameter of the first insulating particles and the average diameter of the second insulating particles fall within a range of 100 nm to 500 nm or a range of 100 nm to half a width of opening of the trench.

16. (Currently Amended) A semiconductor device, comprising:

a semiconductor substrate with a trench, the semiconductor substrate comprising a first semiconductor layer of a first conductivity type and a second semiconductor layer disposed above the first semiconductor layer, and the second semiconductor layer including

a first impurity diffusion region of the first conductivity type,

a second impurity diffusion region of a second conductivity type, the second impurity diffusion region and the trench sandwiching the first impurity diffusion region,

a base region of the second conductivity type which faces the first semiconductor layer with the first and second impurity diffusion regions interposed therebetween and is spaced apart from the trench, and

a source region of the first conductivity type which faces the first semiconductor layer with the base region and the second impurity diffusion region interposed therebetween and is spaced apart from the first impurity diffusion region;
and

a particulate insulating layer filling at least a lower portion of the trench and comprising insulating particles and an insulating binder that bonds the insulating particles together, the insulating particles and the insulating binder forming a network structure, wherein an average diameter of the insulating particles falls within a range of 100 nm to 500 nm or a range of 100 nm to half a width of opening of the trench;

a gate electrode facing a portion of the base region interposed between the first impurity diffusion region and the source region;

a gate insulating film interposed between the gate electrode and the base region;

a source electrode covering the source region; and

a drain electrode covering the first semiconductor layer, the drain and source electrodes sandwiching the semiconductor substrate.

17. (Original) The device according to claim 16, further comprising a barrier insulating layer on a sidewall and a bottom surface of the trench.

18. (Canceled).

19. (Canceled).

20. (Canceled).

21. (Original) A semiconductor device, comprising:
a semiconductor substrate with a trench; and
a particulate insulating layer filling at least a lower portion of the trench and including first and second particulate insulating layers, the first particulate insulating layer comprising first insulating particles with no binder, and the second particulate insulating layer covering an upper surface of the first particulate insulating layer and comprising second insulating particles and an insulating binder.

22. (Original) The device according to claim 21, further comprising a barrier insulating layer on a sidewall and a bottom surface of the trench.

23. (Original) The device according to claim 21, further comprising a reflowable dielectric layer covering an upper surface of the second particulate insulating layer, the first and second insulating particles being stable at a melting point or a softening point of the reflowable dielectric layer.

24. (Original) The device according to claim 23, further comprising a cap insulating layer covering an upper surface of the reflowable dielectric layer and having a melting point or a softening point higher than the melting point or the softening point of the reflowable dielectric layer.

25. (Original) The device according to claim 21, wherein an average diameter of the first and second insulating particles falls within a range of 100 nm to 500 nm or a range of 100 nm to half a width of opening of the trench.

26. (Original) The device according to claim 4, wherein an upper surface of the cap insulating layer is flush with an upper surface of the semiconductor substrate.

27. (Canceled).

28. (Previously Presented) The device according to claim 3, wherein the barrier insulating layer is made of a material selected from the group consisting of silicon oxide, silicon nitride, and a mixture thereof.

29. (Previously Presented) The device according to claim 9, wherein the barrier insulating layer is made of a material selected from the group consisting of silicon oxide, silicon nitride, and a mixture thereof.

30. (Previously Presented) The device according to claim 17, wherein the barrier insulating layer is made of a material selected from the group consisting of silicon oxide, silicon nitride, and a mixture thereof.

31. (Previously Presented) The device according to claim 22, wherein the barrier insulating layer is made of a material selected from the group consisting of silicon oxide, silicon nitride, and a mixture thereof.

32. (Canceled)

33. (Currently Amended) The device according to claim 8, wherein the semiconductor substrate comprises a first semiconductor layer of a first conductivity type, and a second semiconductor layer disposed above the first semiconductor layer, the second semiconductor layer including:

a first impurity diffusion region of the first conductivity type;

a second impurity diffusion region of a second conductivity type, the second impurity diffusion ~~layer~~ region and the trench sandwiching the first impurity diffusion ~~layer~~ region;

a base region of the second conductivity type which faces the first semiconductor layer with the first and second impurity diffusion regions interposed therebetween and is spaced apart from the trench; and

a source region of the first conductivity type which faces the first semiconductor layer with the base region and the second impurity diffusion region interposed therebetween and is spaced apart from the first impurity diffusion region,

wherein the device further comprises:

a gate electrode facing a portion of the base region interposed between the first impurity diffusion region and the source region;

a gate insulating film interposed between the gate electrode and the base region;

a source electrode covering the source region; and

a drain electrode covering the first semiconductor layer, the drain and source electrodes sandwiching the semiconductor substrate.

34. (Canceled)

35. (Currently Amended) The device according to claim 21, wherein the semiconductor substrate comprises a first semiconductor layer of a first conductivity type, and a second semiconductor layer disposed above the first semiconductor layer, the second semiconductor layer including:

- a first impurity diffusion region of the first conductivity type;

- a second impurity diffusion region of a second conductivity type, the second impurity diffusion ~~layer~~ region and the trench sandwiching the first impurity diffusion ~~layer~~ region;

- a base region of the second conductivity type which faces the first semiconductor layer with the first and second impurity diffusion regions interposed therebetween and is spaced apart from the trench; and

- a source region of the first conductivity type which faces the first semiconductor layer with the base region and the second impurity diffusion region interposed therebetween and is spaced apart from the first impurity diffusion region,

- wherein the device further comprises:

- a gate electrode facing a portion of the base region interposed between the first impurity diffusion region and the source region;

- a gate insulating film interposed between the gate electrode and the base region;

- a source electrode covering the source region; and

- a drain electrode covering the first semiconductor layer, the drain and source electrodes sandwiching the semiconductor substrate.